AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A nonvolatile semiconductor memory cell comprising:

a semiconductor substrate;

a stacked-gate structure that includes a tunnel insulation film, a floating gate electrode, an inter-electrode insulation film and a control gate electrode, which are stacked on the semiconductor substrate, the inter-electrode insulation film having a three-layer structure that includes a first oxidant barrier layer, an intermediate insulation layer and a second oxidant barrier layer; and

gate side-wall insulation films formed on both side surfaces of the stacked-gate structure,

wherein [[the]] a thickness of the gate side-wall insulation film increases, at a side portion of the floating gate electrode, from the inter-electrode insulation film side toward the tunnel insulation film side, and the width of the floating gate electrode in a channel length direction decreases from the inter-electrode insulation film side toward the tunnel insulation film side,

wherein a width (Q) of the floating gate electrode in the channel length direction is 50 nm or less on a surface of the tunnel insulation film, and a distance (S) between an end portion of one of the gate side-wall insulation films, which end portion is located on a side opposed to the floating gate electrode, and an end portion of the other gate side-wall insulation film, which end portion is located on a side opposed to the floating

gate electrode, is 1.3 or more times as great as the width (Q) of the floating gate electrode in the channel length direction, and

wherein a portion of the floating gate contacts the inter-electrode insulation film, and a length (P) of the portion of the floating gate satisfies:

$Q < P < S$.

2. (Cancelled)

3. (Original) The nonvolatile semiconductor memory cell according to claim 1, wherein the inter-electrode insulation film has as substantially flat structure, and an area of the tunnel insulation film, which contacts the floating gate electrode, is 70% or less of an area of the inter-electrode insulation film, which contacts the floating gate electrode.

4. (Original) The nonvolatile semiconductor memory cell according to claim 1, wherein the first and second oxidant barrier layers are formed of one of a silicon nitride film, a silicon oxynitride film, a titanium nitride film and a tungsten nitride film.

5. (Original) The nonvolatile semiconductor memory cell according to claim 1, wherein the gate side-wall insulation films comprise a first side-wall insulation film that is provided on a side surface of the floating gate electrode, and a second side-wall insulation film that is provided on a side surface of the control gate electrode.

6. (Currently Amended) The nonvolatile semiconductor memory cell according to claim [[1]] 5, wherein the control gate electrode has a two-layer structure that comprises a high-resistance lower layer and a low-resistance upper layer.

7. (Original) The nonvolatile semiconductor memory cell according to claim 6, wherein the control gate electrode lower layer is formed of polysilicon and the control gate electrode upper layer is formed of silicide.

8. (Original) The nonvolatile semiconductor memory cell according to claim 6, wherein an area where an upper surface of the control gate electrode lower layer contacts a lower surface of the control gate electrode upper layer is substantially equal to an area where a lower surface of the control gate electrode lower layer contacts the inter-electrode insulation film.

9. (Original) The nonvolatile semiconductor memory cell according to claim 6, wherein the second side-wall insulation film is thin at upper and lower surfaces of the control gate electrode lower layer, and thick at a central part of the control gate electrode lower layer.

10. (Original) The nonvolatile semiconductor memory cell according to claim 1, wherein a device isolation insulation film is buried at a side surface of the floating gate electrode in a channel width direction.

11. (Cancelled)

12. (Withdrawn) A method of manufacturing a nonvolatile semiconductor memory cell, comprising:

forming a tunnel insulation film on a semiconductor substrate;

forming on the tunnel insulation film a first conductive layer that becomes a floating gate electrode;

forming on the first conductive layer an inter-electrode insulation film that includes a first oxidant barrier layer, which suppresses passage of oxidant, an

intermediate insulation layer, and a second oxidant barrier layer, which suppresses passage of oxidant;

forming on the inter-electrode insulation film a second conductive layer that becomes a control gate electrode;

forming a stacked-gate structure by selectively etching the first conductive layer, the second conductive layer and the inter-electrode insulation film; and

forming gate side-wall insulation films on side parts of the floating gate electrode by oxidizing or oxynitriding side surfaces of the stacked-gate structure, each of the gate side-wall insulation films having a thickness increasing from the inter-electrode insulation film side toward the tunnel insulation film side.

13. (Withdrawn) The method according to claim 12, wherein a third oxidant barrier layer is formed on the second conductive layer, prior to formation of the gate side-wall insulation films.

14. (Withdrawn) The method according to claim 12, wherein a third oxidant barrier layer is formed on the second conductive layer, prior to formation of the gate side-wall insulation films, and oxidation or oxynitridation is performed to form the gate side-wall insulation films in a state in which the third oxidant barrier layer is present on the second conductive layer.

15. (Withdrawn) The method according to claim 14, wherein the third oxidant barrier layer is removed after formation of the gate side-wall insulation films, and a third conductive layer having a lower resistance than the second conductive layer is formed on the second conductive layer.

16. (Withdrawn) The method according to claim 12, wherein after formation of the gate side-wall insulation films, source/drain diffusion layers are formed by implanting dopant ions in the semiconductor substrate, using the gate side-wall insulation films as a mask.

17. (Withdrawn) The method according to claim 12, wherein the inter-electrode insulation film has as substantially flat structure, and an area of the tunnel insulation film, which contacts the floating gate electrode, is 70% or less of an area of the inter-electrode insulation film, which contacts the floating gate electrode.

18. (Withdrawn) The method according to claim 12, wherein the conductive layers are thermally oxidized by RTP (Rapid Thermal Process), thereby to form a gate side-wall insulation films.

19. (Withdrawn) A method of manufacturing a nonvolatile semiconductor memory cell, comprising:

forming a tunnel insulation film on a semiconductor substrate;

forming on the tunnel insulation film a first conductive layer that becomes a floating gate electrode;

forming on the first conductive layer an inter-electrode insulation film that includes a first oxidant barrier layer, which suppresses passage of oxidant, an intermediate insulation layer, and a second oxidant barrier layer, which suppresses passage of oxidant;

forming on the inter-electrode insulation film a second conductive layer that becomes a control gate electrode lower-layer;

forming a third oxidant barrier layer on the second conductive layer;

forming a stacked-gate structure by selectively etching the first conductive layer, the second conductive layer, the inter-electrode insulation film and the third oxidant barrier layer;

forming first gate side-wall insulation films on side parts of the floating gate electrode and second gate side-wall insulation films on side parts of the control gate electrode lower-layer by oxidizing or oxynitriding side surfaces of the stacked-gate structure, each of the first gate side-wall insulation films having a thickness increasing from the inter-electrode insulation film side toward the tunnel insulation film side, and each of the second gate side-wall insulation films having a thickness decreasing from a central part thereof toward the oxidant barrier layers; and

removing the third oxidant barrier layer and then forming on the control gate electrode lower-layer a control gate electrode upper-layer that has a lower resistance than the control gate electrode lower-layer.

20. (Currently Amended) A memory card comprising:

a memory chip including a plurality of nonvolatile memory cells, and a controller that controls the memory chip, the memory chip and the controller being mounted on a single wiring board,

wherein the memory cell comprises:

a stacked-gate structure that includes a tunnel insulation film, a floating gate electrode, an inter-electrode insulation film and a control gate electrode, which are stacked on a semiconductor substrate, the inter-electrode insulation film having a three-layer structure that includes a first oxidant barrier layer, an intermediate insulation layer and a second oxidant barrier layer; and

gate side-wall insulation films formed on both side surfaces of the stacked-gate structure[[,]] ;

wherein [[the]] a thickness of the gate side-wall insulation film increases, at a side portion of the floating gate electrode, from the inter-electrode insulation film side toward the tunnel insulation film side, and the width of the floating gate electrode in a channel length direction decreases from the inter-electrode insulation film side toward the tunnel insulation film side,

wherein a width (Q) of the floating gate electrode in the channel length direction is 50 nm or less on a surface of the tunnel insulation film, and a distance (S) between an end portion of one of the gate side-wall insulation films, which end portion is located on a side opposed to the floating gate electrode, and an end portion of the other gate side-wall insulation film, which end portion is located on a side opposed to the floating gate electrode, is 1.3 or more times as great as the width (Q) of the floating gate electrode in the channel length direction; and

wherein a portion of the floating gate contacts the inter-electrode insulation film, and a length (P) of the portion of the floating gate satisfies:

$$Q < P < S.$$